REMARKS

Please charge any required fees and credit any overpayments to Deposit Account No. 50-2888. Any required extension of time for submitting the present response is hereby requested, if needed. Applicants claim small entity status.

Claims **1, 8, 9, 20-24,** and **31-33** and **36** were rejected under 35 U.S.C. 103(a) as being unpatentable over Hasley et al. (USPN 5,892,682) in view of Dangelo et al. (USPN 5,493,508). Claims **2-4, 10-19, 23, 27-30** and **37-50** were rejected under 35 U.S.C. 103(a) as being unpatentable over Hasley et al. in view of Dangelo et al. and further in view of Navabi, "VHDL: Analysis and Modeling of Digital Systems."

Applicants thank the Examiner for indicating the allowability of the subject matter of claims **5-7** and **25**. The Examiner's rejections are traversed below.

35 U.S.C. §103

The Office Action stated that "Hasley did not explicitly teach establishing a set of hardware description language models for the cores, each hardware description language model implementing an internal logic of one of the cores; and generating hardware description language core interconnection code for interconnecting the hardware description language models according to the central specification, to generate a hardware description model of the circuit. Dangelo demonstrated that it was known at the time of invention to utilize circuit design system, which provide both software modeling (column 3, lines 55-59) and hardware modeling (column 3, lines 45-54) of cores/modules interchangeably (column 3, lines 60-61). It would have been obvious [...] to implement the modular circuit design of Hasley with modeling in both software and hardware descriptions as found in Dangelo's teaching and thus generate interconnection code for both (hardware and software models) to fulfill modeling of the circuit as previously discussed by Hasley. This implementation would have been obvious because one of ordinary skill in the art would be motivated to provide a well defined design of a modular circuit design (Dangelo: column 3, lines 33-45)."

Applicants respectfully submit that the Office Action has not established a *prima facie* case of unpatentability for the present claims. A *prima facie* case of obviousness requires establishing three elements: the prior art reference (or references when combined) must teach or suggest all the claim limitations; there must be some suggestion or motivation, either in the

references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; and finally, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination must be found in the prior art, and not based on applicant's disclosure. MPEP 2142.

Applicants submit that, first, Dangelo et al. do not cure the acknowledged deficiencies of Hasley et al., and thus the Office Action has not established that the combined references teach all claim limitations; second, even if a skilled artisan would have attempted to combine the teachings of Hasley et al. and Dangelo et al., such a combination would not have yielded the subject matter of claim 1; and third, the motivation advanced by the Office Action appears to originate from hindsight, rather than a fair reading of the teachings of Dangelo et al. Each argument is treated below in turn.

I. Combined references must teach all claim limitations: Dangelo et al. do not cure the deficiencies of Hasley et al. set forth in the Office Action

A *prima facie* case of obviousness requires establishing that the prior art references, when combined, must teach or suggest all the claim limitations. Applicants submit that Dangelo et al. fail to cure the deficiencies of Hasley et al. acknowledged in the Office Action, because Dangelo et al. do not supply the claim limitations acknowledged to be missing from Hasley et al.

Claim 1 requires establishing a set of hardware description language (HDL) models for a plurality of cores, each HDL model implementing an internal logic of one of the cores; and generating HDL interconnection code for interconnecting the HDL models according to the recited central specification, which designates the plurality of cores and a plurality of interconnections between the cores.

Dangelo et al. describe a methodology for generating structural descriptions of complex digital devices from high-level descriptions and specifications (Abstract). Dangelo et al. provide a succinct description of a number of steps involved in a method of their invention at column 5, lines 20-67 ("Disclosure of the Invention" section, which appears to be a summary), and column 9, line 15 through column 10 line 36.. Dangelo et al. describe systems and methods "enabling a designer to create and validate a structural description and physical

implementation of a circuit or system (hereinafter, "device") from a behavior-oriented description using a high-level computer language." Column 5, lines 22-26 of Dangelo et al. In the Dangelo et al. system, "first, the designer specifies the desired behavior of the device in a high-level language, such as VHDL." Exemplary behavioral code is shown in Fig. 12 (block 1212), and is referenced on column 9, lines 20-24 of Dangelo et al. The behavioral model is then used to generate a structural model of the circuit and to physically implement the circuit, as described for example on column 5, lines 35-67, column 9, lines 25-39, and column 11 line 25 through column 13 line 50 of Dangelo et al., and as illustrated for example in Fig. 12.

The behavioral description of Dangelo et al. (see block 1212 in Fig. 12) describes system behavior using VHDL code containing statements such as Begin, If and Else. Dangelo et al. states that, in a behavioral description, "the design is described in sequential program statements similar to a high-level programming language." Column 3, lines 55-58. This behavioral description is not a central specification designating a plurality of cores and a plurality of interconnections between the cores as claimed. Dangelo et al. do not teach establishing a set of hardware description language models for the cores, each hardware description language model implementing an internal logic of one of the cores; and generating hardware description language core interconnection code for interconnecting the hardware description language models according to the central specification to generate a hardware description model of the circuit, as recited in claim 1.

Since a *prima facie* obviousness case requires that all claim limitations be found in the combined cited references, and since Dangelo et al. do not supply the limitations set forth to be missing from Hasley et al., Applicants submit that the Office Action has not established a *prima facie* case of unpatentability for the instant claims.

II. A non-hindsight combination of teachings of Hasley et al. and Dangelo et al. would not have yielded the subject matter of claim 1

Applicants submit that even if a skilled artisan were hypothetically to have attempted to combine the teachings of Hasley et al. with those of Dangelo et al., a non-hindsight combination of the teachings of the two references would not have yielded generating, from a central specification designating a plurality of cores and inter-core connections, both hardware description language core interconnection code for interconnecting hardware description

language core models, and software interconnection code for interconnecting software language core models, as recited in claim 1.

Applicants submit that a skilled artisan hypothetically wishing to combine the teachings of Hasley et al. and Dangelo et al. at most would have applied the Dangelo et al. design technique to a completed behavioral system design, which is the starting point described by Dangelo et al. Such a combination would have produced a low-level structural description of the circuit from a completed behavioral model (the starting point for the Dangelo et al. process), not by interconnecting hardware description models of the cores according to the starting high-level specification designating cores and core interconnections as claimed. Thus, a skilled artisan attempting to combine the teachings of Hasley et al. and Dangelo et al. would not have arrived at the subject matter of claim 1.

III. Read for their true teachings, Dangelo et al. do not provide a suggestion or motivation to make the modifications proposed by the Office Action

The Office Action appears to advance several motivations for making the proposed modifications/additions to Hasley et al. Applicants submit that some of the teachings cited by the Office Action are not specific or relevant enough to have motivated a skilled artisan to make the proposed modifications, while others cannot be fairly found in Dangelo et al. Each potential motivation advanced by the Office Action is treated below in turn.

On page 3, the Office Action stated that the advanced modifications would have been obvious "because one of ordinary skill in the art would be motivated to provide a well-defined design of a modular circuit design (Dangelo: column 3, lines 33-45)." In the section entitled "Response to Arguments" on p. 18-19, the Office Action stated that "First, Hasley disclosed a central specification and software models as previously indicated. Second, Dangelo disclosed hardware models *and* software models being intermixed in some sort of specification (column 3, lines 46-61; in particular last sentence). Third, Dangelo provided motivation in column 3, lines 33-45 by indicating a design/specification must fully encompass all aspects of the final product (system, gates, chips, abstractions, software, and hardware). Thus, [...] Dangelo provided that all elements to be produced (a hardware implementation to a software implementation/simulation) ideally should come from a single source. Additionally, the broadest reasonable interpretation of the claims simply stated that a software model and a hardware model are derived from one source. Dangelo, at least, illustrated that one source can

and has produced both hardware and software models. The claim language is broad enough that this production of models could be at completely different times and have nothing to do with each other."

i. Providing a well-defined design of a modular circuit design (column 3, lines 33-45 of Dangelo et al.)

Applicants submit that a *prima facie* obviousness case requires setting forth some specific motivation or suggestion in the prior art, rather than a stock, generic advantage or purpose. The Federal Circuit has repeatedly warned against the temptation of hindsight reconstruction (see for example *In re Fine*, 837 F.2d 1071, 1075, 5 USPQ 2d 1596, 1600 (Fed. Cir. 1988), *In re Rouffet*, 149 F.3d 1350, 47 USPQ 2d 1453, 1458 (Fed. Cir. 1998), *In re Fritch*, 972 F.2d 1260, 23 USPQ2d 1780 (Fed. Cir. 1992)). If a general motivation were acceptable, then a stock statement that a proposed modification would for example "improve a system" could be used to justify almost any hindsight-based modification of a prior art reference to arrive at the subject of a claim (except, presumably, for modifications that would not improve a system), and the motivation requirement would be effectively eviscerated. The requirement for specificity in the motivation element is a guard against impermissible hindsight reconstruction. While an explicit suggestion to make a particular modification need not be expressly found in the prior art, the proposed motivation to combine must be specific if the motivation requirement is to be meaningful.

A motivation to "provide a well-defined design of a modular circuit" is so generic as to be meaningless. Such a motivation could be used to support hindsight-based reconstructions of almost any claims directed to modular circuit design. It is in effect little more than a motivation to "improve a modular circuit design," and thus it is not sufficient as a motivation to make the highly particularized modifications proposed by the Office Action.

Furthermore, the passage on column 3, lines 33-45 of Dangelo et al. does not provide a suggestion or motivation to make the modifications put forward by the Office Action. Column 3, lines 33-45 of Dangelo et al. contain a general discussion of VHDL: the language is considered to represent an important step forward in design specification languages because the semantics (intent) of the language constructs are clearly specified; VHDL unambiguously describes intended system behavior; the design entity is the primary hardware abstraction in VHDL; a design entity may represent an entire system, a sub-system, a board, a chip, a macro-

cell, a logic gate, or any level of abstraction in between; a configuration can be used to describe how design entities are put together to form a complete design." Applicants submit that it is not at all clear why the above-paraphrased background passage provides a suggestion or motivation to make the modifications suggested by the Office Action, rather than apply the teachings of Dangelo et al. on generating a structural model from a behavior-oriented circuit model.

ii. Hardware and software models intermixed in some sort of specification (column 3, lines 46-61, in particular last sentence, of Dangelo et al.)

On column 3, lines 46-61, Dangelo et al. provide general background on VHDL by stating essentially that VHDL supports three distinct styles for the description of hardware architectures: structural, data-flow, and behavioral. The last sentence of the passage states that "all three styles may be intermixed in a single architecture."

Applicants submit that it is not clear how or why the above-cited general description of VHDL properties would have motivated a skilled artisan to perform the modifications advanced by the Office Action. In particular, it is not clear how or why a teaching that behavioral, data-flow, and structural descriptions may be "intermixed in a single architecture" would have led a skilled artisan to generate software and hardware interconnection code according to a central specification designating a plurality of cores and inter-code connections, to interconnect core software and hardware models, respectively, so as to generate a software and a hardware model of the circuit as claimed. For example, it is not clear why, from a statement that design entities can be represented at various levels of abstraction, a skilled artisan would have been motivated to arrive at the claimed subject matter, rather than apply the teachings of Dangelo et al. to a completed behavioral model as described by Dangelo et al.

iii. A design/specification must fully encompass all aspects of the final product (system, gates, chips, abstractions, software and hardware) (column 3, lines 33-45 of Dangelo et al.).

Applicants have detailed above why the passage on column 3, lines 33-45 of Dangelo et al. does not provide a suggestion or motivation for making the proposed modifications.

iv. All elements to be produced (a hardware implementation to a software implementation/simulation) ideally should come from a single source (the passages of Dangelo et al. cited above).

Applicants submit that it is not at all clear why a skilled artisan, without hindsight, would have understood the above-referenced passages of Dangelo et al. to suggest that all elements to be produced (hardware model and software model) should come from a single source, or that the single source should be a central specification designating cores and core interconnections as claimed. The suggestion that both hardware and software models be derived from a single central specification appears to come from applicants' specification, rather than from the cited teachings of Dangelo et al.

As discussed above in section II, Dangelo et al. describe systems and methods for creating and validating a structural description and physical implementation of a circuit or system from a behavior-oriented description using a high-level computer language. Column 5, lines 22-26 of Dangelo et al. In the teachings of Dangelo et al., the structural description is derived from the behavior-oriented description. It is not clear why the teachings of Dangelo et al. would have motivated a skilled artisan to derive both hardware and software models from a central specification as claimed, rather than derive a structural description from a behavior-oriented description as taught by Dangelo et al.

Finally, the Office Action stated that "the broadest reasonable interpretation of the claims simply stated that a software model and a hardware model are derived from a single source. Dangelo, at least, illustrated that one source can and has produced both hardware and software models." This statement appears to consider the behavior-oriented model of Dangelo et al. to be the referenced single source. Applicants submit that it is absolutely unambiguous that the central specification recited in claim 1 is distinct from the recited completed software model. As discussed above, Dangelo et al. described producing a structural model from a behavioral model, and not a hardware model and a software model from a central specification designating cores and core interconnections as claimed.

With regard to claim 24, applicants note that claim 24 recites software language template code and hardware language template code, and processing the central specification to generate hardware language interconnection code interconnecting the hardware language template code

and software language interconnection code interconnecting the software language template code. The Office Action stated merely that "the limitation of claims 24 [...] correspond to the limitations of computer-implemented method claim 1." Applicants submit that the Office Action has not pointed out teachings in the prior art for each element of claim 24, nor otherwise made a *prima facie* case of unpatentability for claim 24.

Applicants respectfully submit the instant claims to be patentable in view of the prior art of record, and request the Examiner to indicate the allowability of the instant claims in the next Office Action.

Respectfully submitted, Date: 12/27/2004

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